REMARKS

In the first Office Action, the Examiner objected to claims 4 and 8. As suggested by the Examiner, these claims have now been corrected to replace the term "matter" with --material--.

Claims 1-6 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Blalock (5,320,981) and Wu (5,940,731). Blalock teaches a method for forming a sloped contact which utilizes a photoresist mask to etch the edges of a dielectric material and form the desired sloping of the via. As acknowledged by the Examiner, Blalock does not teach or suggest the use of a hard mask material formed on a dielectric material as claimed, nor does he teach or suggest a dielectric material including a pair of shoulders having a hard mask material thereon, where the layer of mask material has a pair of facets.

However, the Examiner asserts that Wu teaches a dielectric layer 14 having a pair of shoulders 34 with a hard mask material 28 (polysilicon layer 52). The Examiner further asserts that Wu teaches a pair of facets and an interconnect material (72) in the via. The Examiner has concluded that it would have been within the scope of one skilled in the art to combine the teachings of Blalock and Wu "to enable formation of the interconnect structure." However, this is not sufficient to establish a *prima facie* case of obviousness as the Examiner has provided no substantive evidence or reasoning as to how or why one skilled in the art would have been led to combine the teachings of the references. See MPEP 2143.01 and *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

Further, applicant submits that there is nothing in either Blalock or Wu which would motivate one to combine their teachings. Blalock teaches a method of forming a via by re-depositing <u>dielectric</u> material during etching to form sidewall spacers. See Figs. 5 and 6, and claim 1 (f). In contrast, Wu teaches forming a via by a second deposition of polysilicon to form sidewalls of polysilicon which are *conductive*, <u>not</u> dielectric. There is no teaching in either Blalock or Wu which would suggest to one

skilled in the art to make Blalock's sidewall spacers from a separate deposition of a conductive material.

In addition, both Wu and Blalock teach methods which differ substantially from that of the present invention. In the present invention, the hard mask material is formed on the conductive layer and maintained in place during the method of forming the precursor. In contrast, Blalock teaches removing photoresist mask 16 prior to facet etching his dielectric layer 14. Blalock teaches no shoulders on his dielectric material, nor does he teaching forming facets on a hard mask layer. Rather, Blalock teaches facet etching his dielectric layer 14. See col. 4, lines 56-59.

Further, as pointed out in the background portion of applicant's specification, the photoresist material used by Blalock results in the deposition of particles in the resulting via and conductive material which adversely affect subsequent step coverage and conductivity of the resulting semiconductor device.

With regard to Wu, he forms polysilicon spacers (shoulders) by depositing a second poly-silicon layer 28 and then anisotropically etching. The shoulders of the present invention are formed by re-depositing hard mask material which was previously removed in an etch step. See the specification at page 10, lines 3-13.

Accordingly, there is no motivation to combine the teachings of the references, and even if combined, they would not suggest the claimed semiconductor device precursor.

Claim 7 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Blalock and Wu and further in view of Trivedi et al. (5,847,463). The Examiner acknowledges that the combined teachings of Blalock and Wu do not teach or suggest that the hard mask material comprises a titanium-tungsten alloy as claimed. The Examiner points to col. 5, lines 33-37 of Trivedi et al., which teaches that titanium-tungsten may be used as a hard mask layer.

However, applicant first wishes to point out that Trivedi et al. issued after the effective filing date of this application (February 5, 1998). As Trivedi et al. qualifies as

prior art only under section 102(e) and was, at the time the invention was made, commonly assigned to the assignee of the claimed invention (Micron Technology, Inc.), it cannot be cited as a prior art reference in an obviousness rejection. See 35 U.S.C. §103(c).

And, as pointed out above, the combined teachings of Blalock and Wu do not teach or suggest the claimed invention. Claim 7 is patentable.

For all of the above reasons, applicants submit that claims 1-8, as amended, are patentable over the cited references. Early notification of allowable subject matter is respectfully requested.

Respectfully submitted,

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